#8 Affidavit

2/25/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

Applicant(s): Jonathan H. Fischer
Case: 41
Serial No.: 10/002,028
Filing Date: November 15, 2001
Group: 2828
Examiner: Leith A. Al-Nazer

Title: Optical Source Driver with Improved Input Stage

AFFIDAVIT UNDER 37 C.F.R. §1.131

I, the undersigned, hereby declare and state as follows:

1. I am the sole inventor of the invention described and claimed in the above-referenced U.S. patent application.

2. On or about January 24, 2001, I prepared a description of the invention, relating to an optical source driver with an improved input stage, that is the subject of the above-referenced application. I initialed and dated the description. I included in the description a number of computer-generated schematic diagrams, which are dated January 24, 2001. A copy of the description is attached hereto as Exhibit 1.

3. The description in Exhibit 1 evidences conception of an invention falling within one or more of the claims of the application.

4. I continued to work on the invention in the spring and early summer of 2001.

5. In the early summer of 2001, I brought the invention to the attention of the legal department of Agere Systems Inc. ("Agere") for consideration for possible patent protection.

6. Agere subsequently engaged an outside counsel patent attorney, Joseph B. Ryan of Ryan, Mason & Lewis, LLP, to prepare and file a patent application on the invention. In the late summer and fall of 2001, I worked with Mr. Ryan in preparing the application, and the application was filed on November 15, 2001.

7. All statements made herein of my own knowledge are true, and all statements made on information and belief are believed to be true.

8. I understand that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 U.S.C. §1001, and may jeopardize the validity of the application or any patent issuing thereon.

Date: FEB. 7, 2003

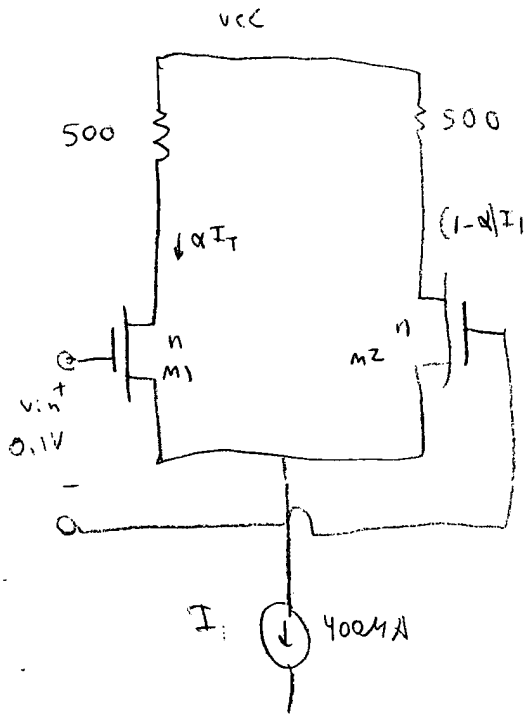
Jonathan H. Fischer

MOS DIFF PAIR INPUT FOR THE CLOCK DRIVER

J.N. FISCHER

1/24/2001

SUMMARY: BY GOING TO A UNITY GAIN INPUT DIFFERENTIAL PAIR, THE CMOS DEVICES ARE SMALL ENOUGH NOT TO LIMIT CIRCUIT SPEED WHILE AVOIDING THE 2V DIFFERENTIAL INPUT VOLTAGE CONSTRAINT WITH A SiGe BIPOLAR INPUT STAGE.



CONSTRAINTS: DIFF PAIR TO STEER > 0.9 × I_T WITH VIN = ± 0.1V

$$v_{in} = V_{gs_1} - V_{gs_2} \qquad V_{gs} = V_T + \sqrt{\frac{2I}{K_P(\frac{W}{L})}}$$

$$= V_T + \sqrt{\frac{2I\alpha}{K_P\frac{W}{L}}} - V_T - \sqrt{\frac{2I(1-\alpha)}{K_P\frac{W}{L}}}$$

$$V_{in} = \sqrt{\frac{2I}{K_P\frac{W}{L}}}\left[\sqrt{\alpha} - \sqrt{1-\alpha}\right]$$

$$= b$$

FIG. 1 SHOWS A PLOT OF $b = \sqrt{\alpha} - \sqrt{1-\alpha}$

FIG. 2 IS AN EXPANDED VIEW OF THE REGION WHERE 90% OF I IS STEERED TO ONE LEG.

$b(0.1) = -0.632$
$b(0.9) = 0.632$

POINT TAKEN FROM SPLUS CALCULATION WHERE $\alpha = 0.1, 0.9$ RESPECTIVELY.

$V_{in} = 0.632\sqrt{\frac{2I}{k_p \frac{W}{L}}}$ TO STEER 90% OF I TO ONE SIDE OF THE DIFFERENTIAL PAIR (1)

EQU (1) CAN NOW BE REARRANGED TO FIND $\frac{W}{L}$ FOR A GIVEN I & VIN

$V_{in} = 100\,mV$ TO MEET OPTO SINGLE-ENDED DRIVE SPEC OF 100 mV PEAK

$$V_{in}^2 = [0.632]^2 \frac{2I}{k_p \frac{W}{L}}$$

$$\frac{W}{L} = \frac{2I}{k_p} \frac{[0.632]^2}{V_{in}^2}$$

$$= \frac{2[400\mu A]}{[100\mu A/V^2][0.1V]^2}$$

$$\frac{W}{L} = \frac{8}{0.01} = 800$$

FOR L = 0.32MM [$L_{eff_{max}} = 0.36$ AFTER PROCESSING]

$W \geq 800 \times 0.36MM$

$\boxed{W \geq 288MM}$

NOTE: IF $V_{IN_{MIN}}$ WAS 200 mV, W_{MIN} WOULD BE $\frac{1}{4}$ THIS SIZE (72MM FOR 200 mV INPUT VOLTAGE).

Fig. 3 show the first test circuit.

AS CAN BE SEEN IN Fig 4, THE PARASITIC CAPITANCE FROM M11 & M12 KILLED THE RESPONSE. THE TIME CONSTANT IS ≈ 4 CLOCK PERIODS [AT 2.5 Gb/s].

TAKING A DIFFERENT VIEW, THE INPUT DIFF AMP SERVES TWO KEY FUNCTIONS; 1, ISOLATE THE SECOND AMP FROM THE INPUT COMMON MODE SIGNAL SO THE STAGE CAN

USE THE LEVEL SHIFTING DIODE, Q10, TO ELIMINATE ONE SET OF EMITTER FOLLOWERS IN THE CLOCK DRIVER OUTPUT STAGE [REDUCE COMMON MODE RINGING]

2/ IF POSSIBLE, USE CMOS INPUTS TO ALLOW RAIL-TO-RAIL INPUT SWING WITHOUT RISKING BI-POLAR EMITTER-BASE BREAK DOWN,
THE CMOS INPUTS ALSO OPENUP THE POSSIBILITY OF USING ≈ STANDARD ESD PROTECTION.

SINCE THE BULK OF ANY SIGNAL GAIN CAN BE LEFT TO THE Q8-Q9 DIFF PAIR, REDUCE THE WIDTH OF M11&M12 FOR UNITY DIFFERENTIAL GAIN, (FOR A 100mV RECALL THAT THE ONLY REASON THE FIRST DIFF PAIR WAS ADDED TO THE CLOCK BUFFER WAS TO PROVIDE THE SECOND AMP WITH A WELL KNOWN COMMON MODE SIGNAL THAT IS 1-VBE LOWER THAN THE ONE DIFFAMP CASE.

THE Z417K4A 2.5Gb/s TRANSCEIVER SPECIFICATION:
CML INPUT SIGNAL RANGE: 300 mVp-p [150 mV peak] to 1.6Vp-p [0.8Vp] DIFFERENTIAL
AND 150 mVp-p [75mVpeak] to 800mVp-p [0.4Vp] SINGLE-ENDED - SYSTEM SPECS ONLY GUARENTEED FOR DIFFERENTIAL INPUT.

FOCUSING ON THE SMALL DIFF. DRIVE CASE,
FIG. 5 SHOWS THE RESPONSE FOR 100mV PEAK DRIVE WITH M11&M12 SCALED DOWN TO $\frac{24}{0.32}$. THE DIFF PAIR ONLY STEERS $\frac{1}{3}$ THE TAIL CURRENT INSTEAD OF >90% FOR THE ORIGINAL DEVICE SIZES. STILL, IT LOOKS TO BE GOOD ENOUGH.

FIG. 6 SHOWS THE RESPONSE WITH M11&M12 REDUCED TO $\frac{2.0\,mm}{0.32\,mm}$
NOW THE SECOND DIFF PAIR OUTPUT WAS REDUCED BY 3% FROM THAT IN FIG. 5, FOR NOW, KEEP M11=M12 = $\frac{24\,mm}{0.32\,mm}$.
FIG. 7 SHOWS THE REVISED SCHEMATIC.

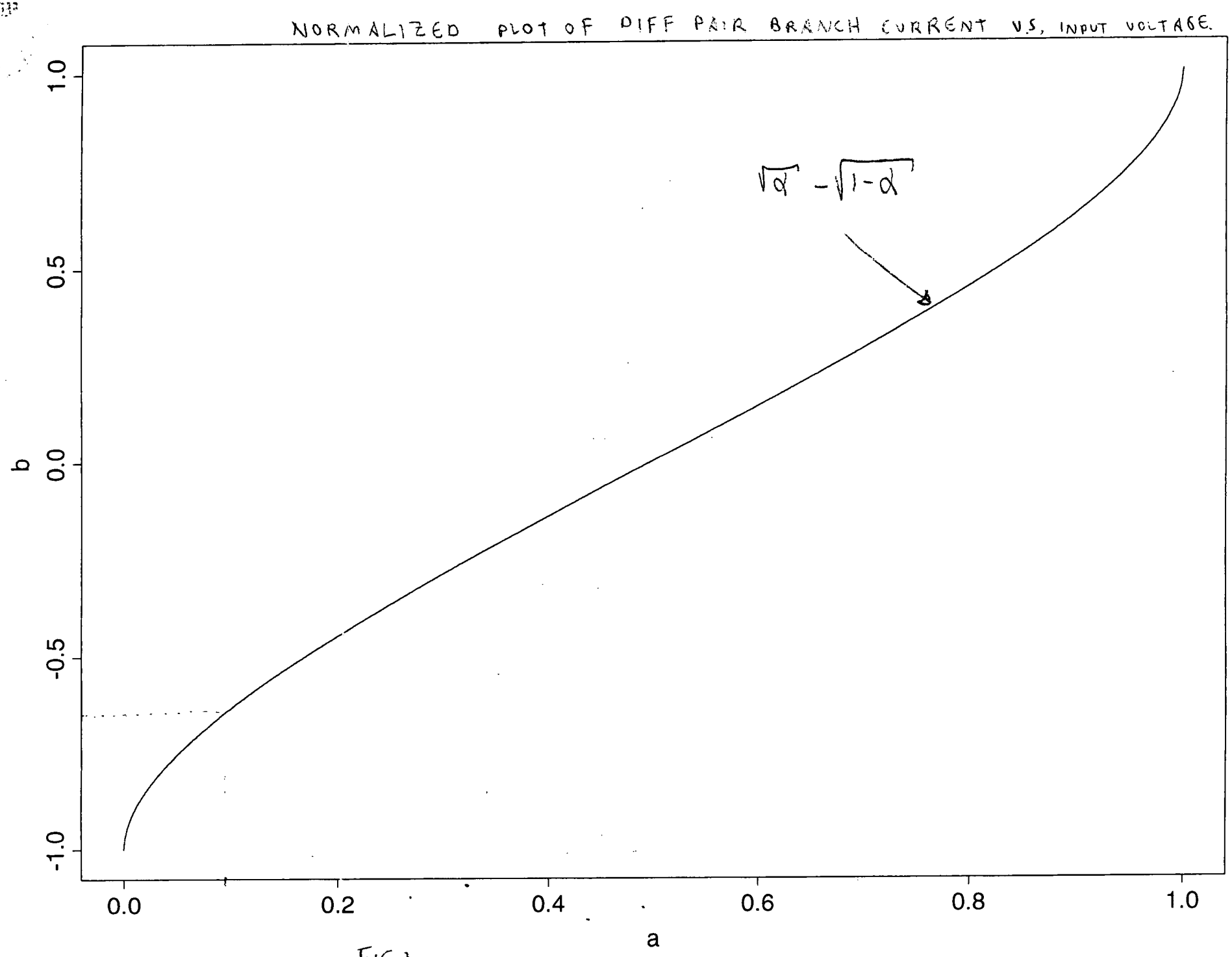

NORMALIZED PLOT OF DIFF PAIR BRANCH CURRENT V.S, INPUT VOLTAGE.
$\sqrt{\alpha} - \sqrt{1-\alpha}$
b
a
1.0
0.5
0.0
-0.5
-1.0
0.0
0.2
0.4
0.6
0.8
1.0

FIG.1

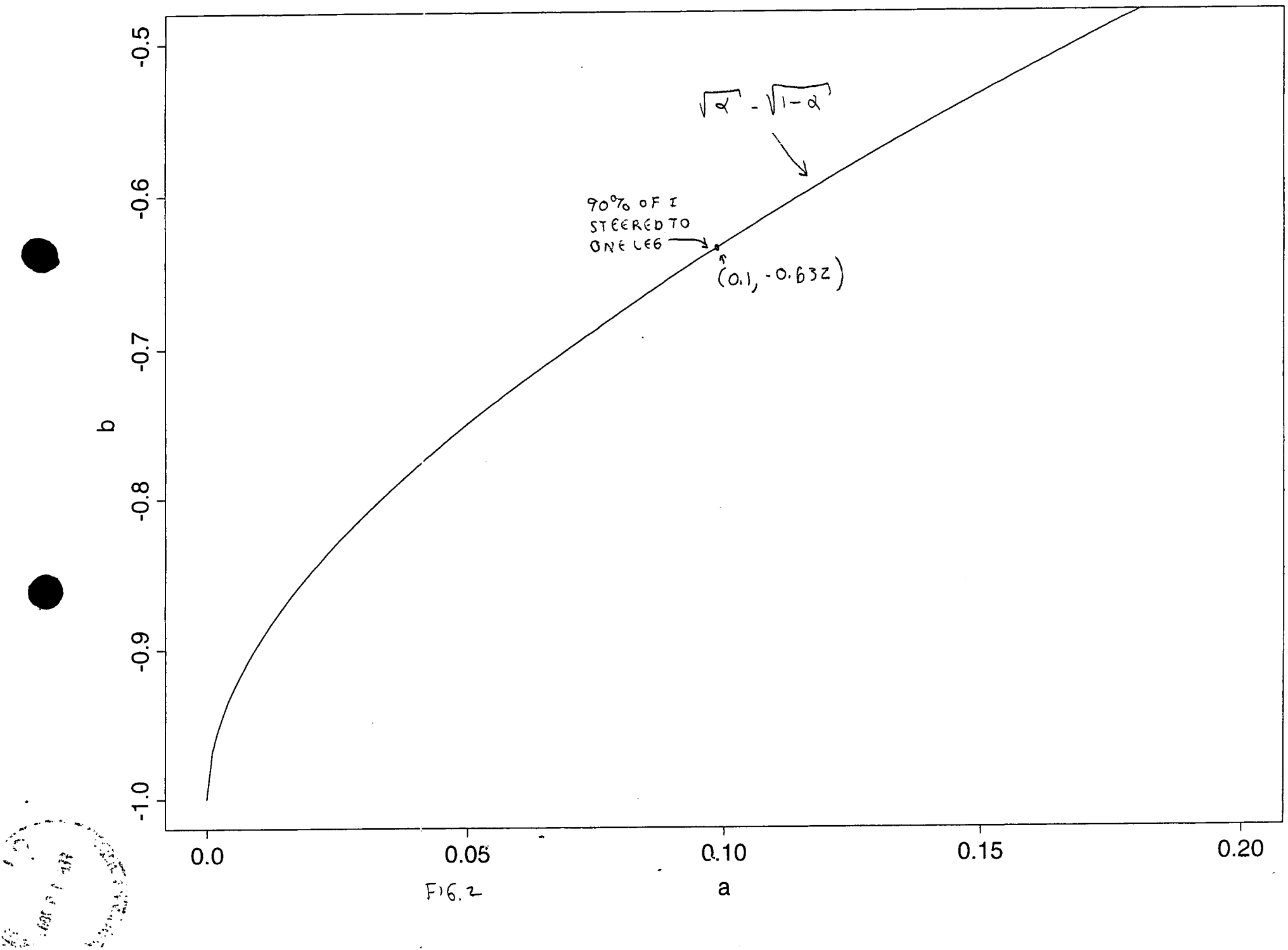
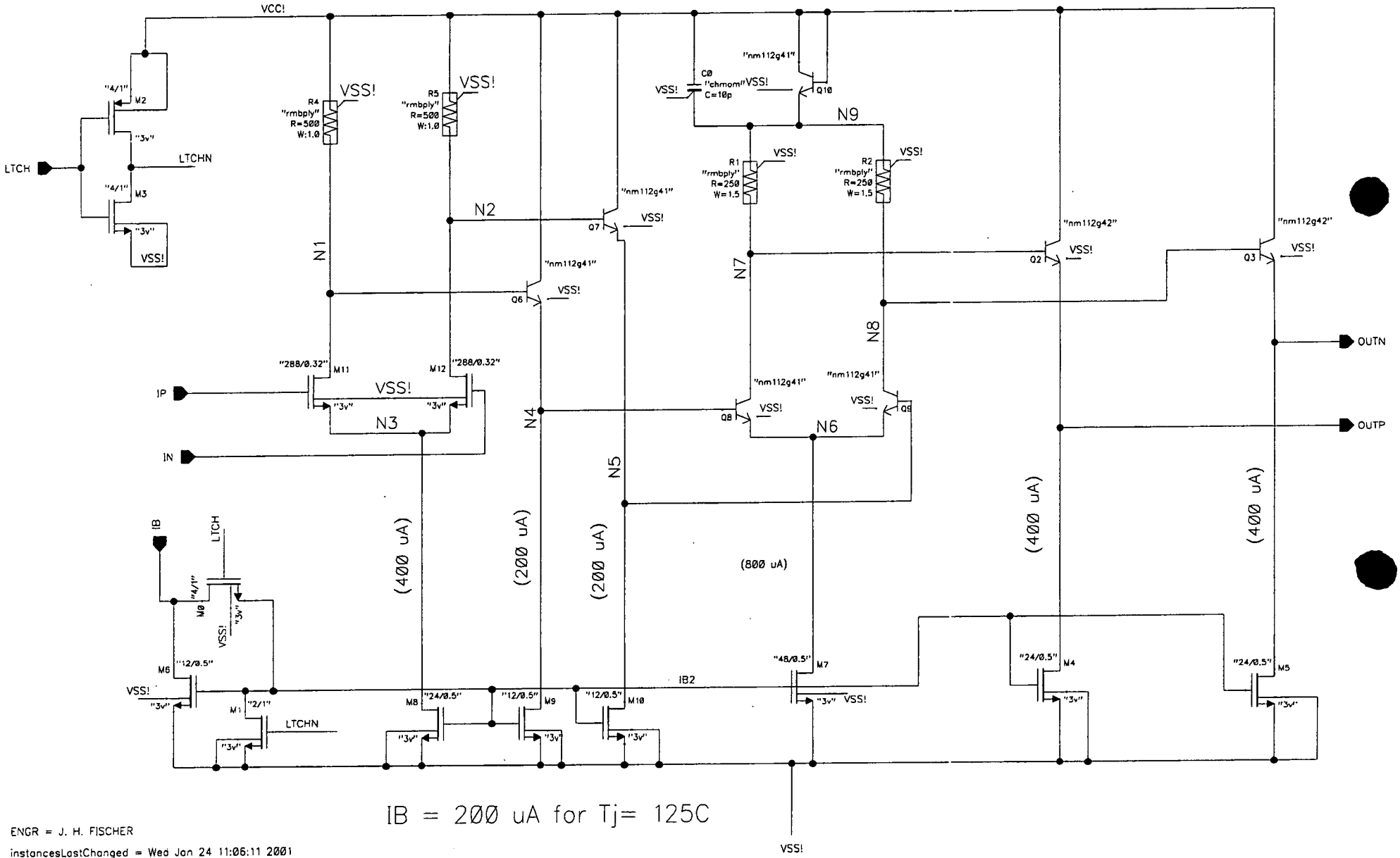

$\sqrt{\alpha} - \sqrt{1-\alpha}$
90% OF I STEERED TO ONE LEG
(0.1, -0.632)
-0.5
-0.6
-0.7
-0.8
-0.9
-1.0
b
0.0
0.05
0.10
0.15
0.20
a

FIG. 2



IB = 200 uA for Tj= 125C

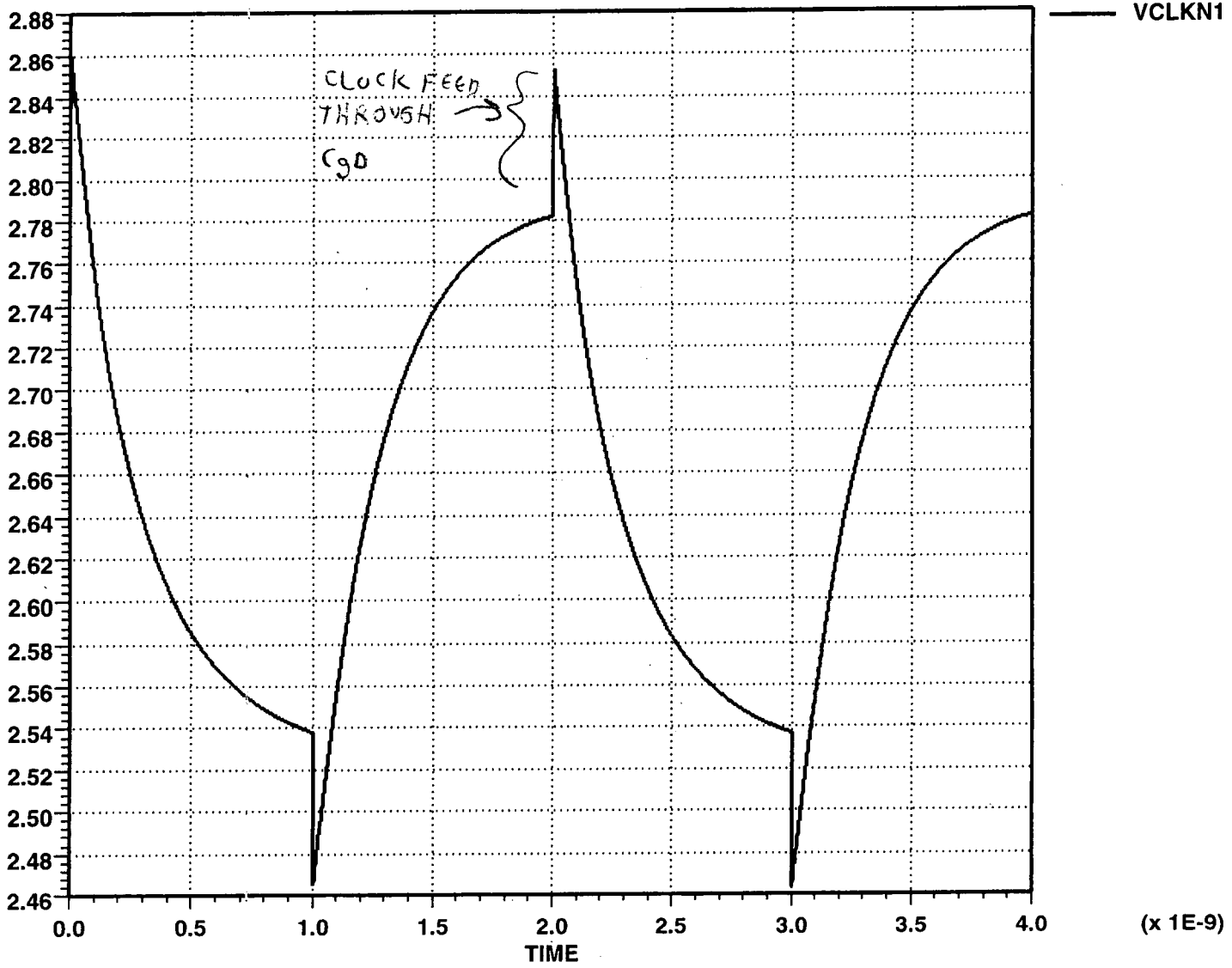
F16, 3

ENGR = J. H. FISCHER
instancesLastChanged = Wed Jan 24 11:06:11 2001
lastSchematicExtraction = Wed Jan 24 11:06:12 2001
libName = TOP_LIBRARY
cellName = clkin3

LTCH: 0 – BYPASS FF, SHUT DOWN CLOCK BUFFI
1 – FF USED, BUFFER ACTIVE

Celerity 2.8.3 RAN 01/24/2001 AT 14:39:22 S# 2873 125 DEG C

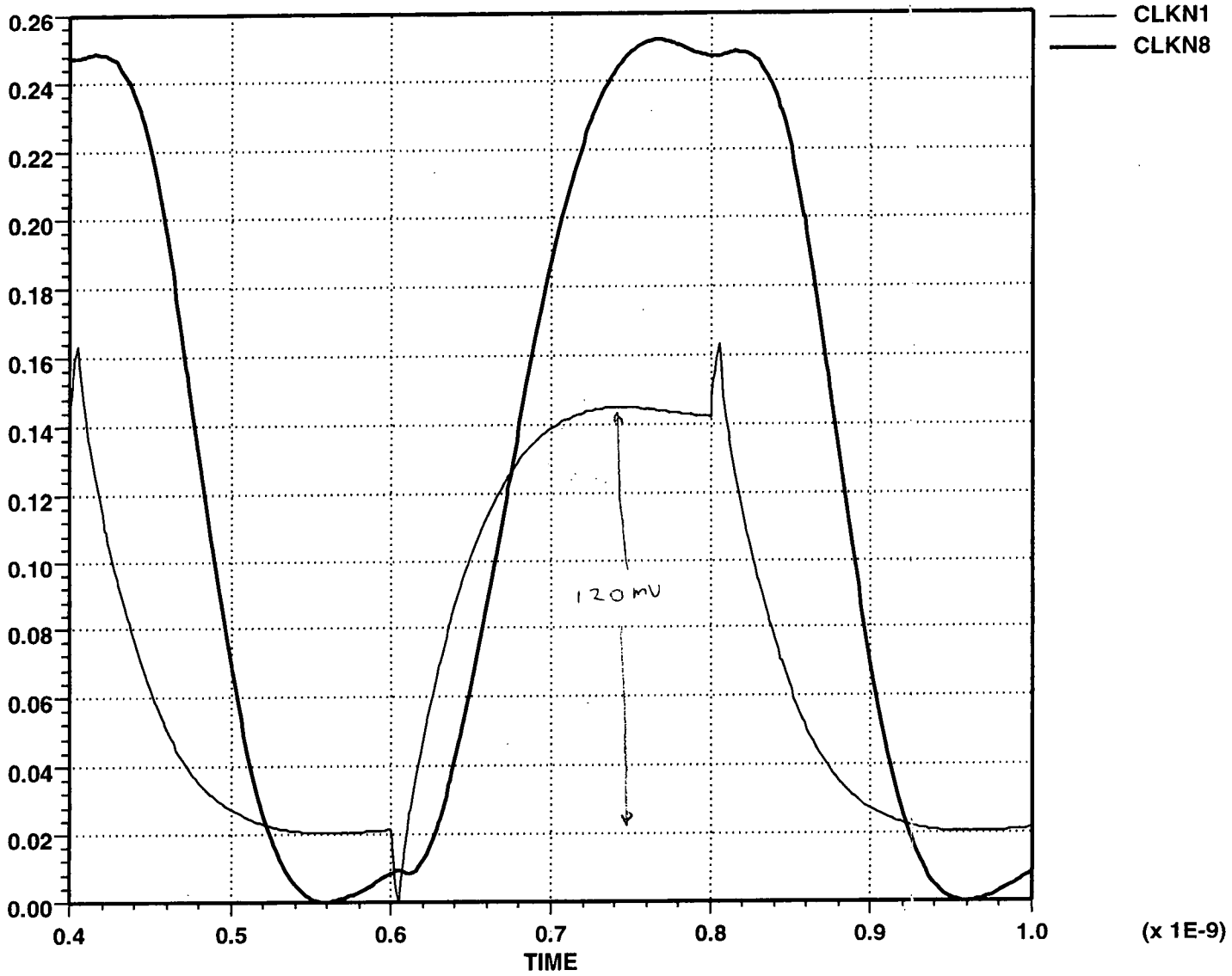
wc slow,VCC=2.8,cp included,IBMOD=60mA,f-f in, clkin3 $m11 = m12 = \frac{288}{0.32}$



$\zeta = 1NS$ FOR INPUT STAGE

Fig. 4

Celerity 2.8.3 RAN 01/24/2001 AT 15:40:18 S# 3305 125 DEG C
wc slow,VCC=2.8, clkin3 (M11, M12 = 24/0.32) VIN=100mV peak diff.



0.248
0.240
.008

0.008
0.240

Fig. 5

Celerity 2.8.3 RAN 01/24/2001 AT 17:50:19 S# 3551 125 DEG C

wc slow,VCC=2.8, clkin3 (M11, M12 = 20/0.32) VIN=100mV peak diff.

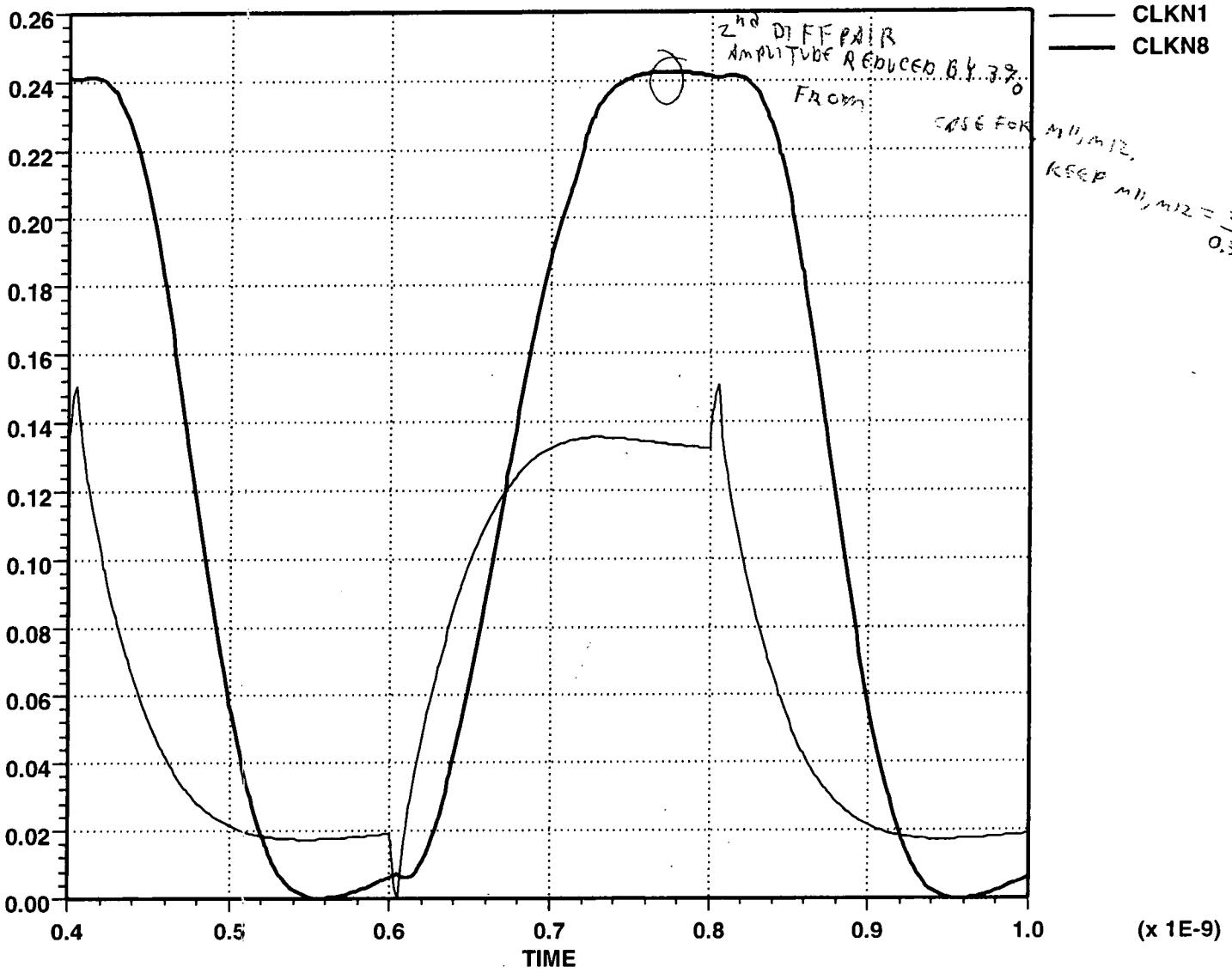
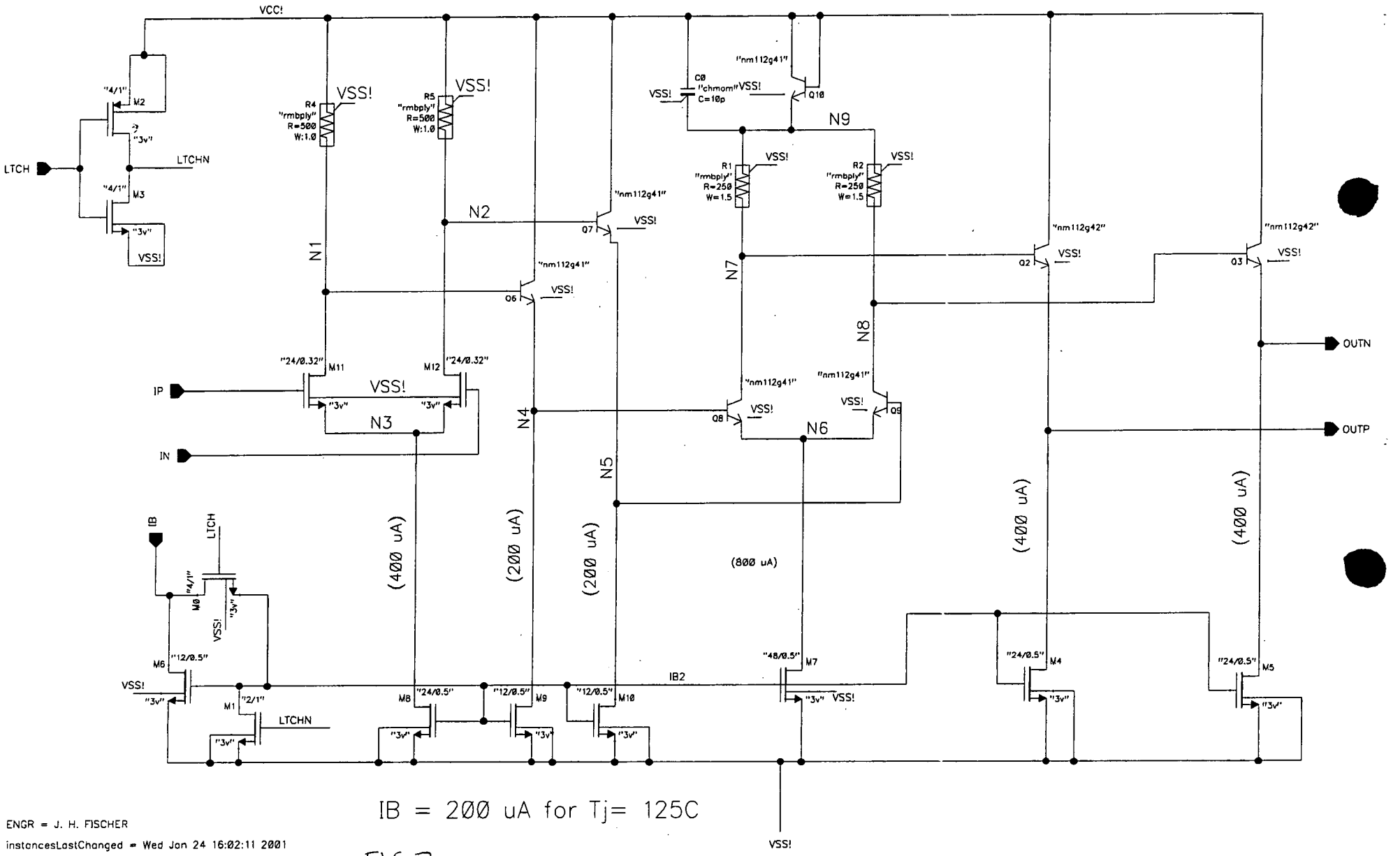


FIG. 6



IB = 200 uA for Tj= 125C

FIG. 7

ENGR = J. H. FISCHER
instancesLastChanged = Wed Jan 24 16:02:11 2001
lastSchematicExtraction = Wed Jan 24 16:02:11 2001
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cellName = clkin3

LTCH: 0 – BYPASS FF, SHUT DOWN CLOCK BUFFE
1 – FF USED, BUFFER ACTIVE